

# ARM / i.MX 51

HILF! GmbH Microcomputer-Consulting, Bajuwarenring 17, 82041 Oberhaching/München  
Tel.: +49 (89) 61 37 90 - 0, Fax: +49 (89) 62 52 14 5

Web: [www.hilf.de](http://www.hilf.de)  
Email: [info@hilf.de](mailto:info@hilf.de)

## Target group

Application Software and system engineers who need to come up to speed quickly on how to design with this architecture.

## Prerequisites

Due to the high degree of functionality and integration of this device, the student is encouraged to gain some familiarity beforehand by reviewing current Freescale documentation for this product. Introductory level web-based training materials are available at [www.freescale.com/training](http://www.freescale.com/training). Search on i.MX51 for a list of available overview materials.

## Course description

The i.MX51 is a 4-day class lecture covering the main features of the i.MX51 architecture, operation and programming.

This course covers the ARM Cortex A8T platform including programming model exceptions and interrupt handling, interrupt controller, instruction set, Application Processor level 1 and level 2 caches, cross-bar switch, Memory Management Unit (MMU), application processor I/O peripherals, Smart Direct Memory, Access Control, Multi-master Multi-Memory Interfaces (M4IF), Graphics and Image Processing unit (IPU) and system wide integration.

Target Applications: Wireless device running computationally intensive multimedia applications such as portable media players and portable navigation devices. Target devices also include feature rich smart phones, digital video recorders, digital cameras, mobile gaming consoles, mobile multimedia players and many other mobile wireless applications.

## Course material

- course notes

## Course topics

- System Overview
  - Platform Overview
  - ARM Cortex T Platform overview
- System-wide Connectivity
- ARM Cortex A8 Core
  - ARM Cortex A8 Core
  - Instruction Pipe
  - Branch Prediction
  - Programming Model
  - Register Banking
  - Stacking
  - ARM® -Thumb Engines and Switching
  - ARM Instruction Set Overview
- Thumb Programming Model and Instruction Set
- NEON Overview
  - Programming Model
  - Instruction Set
- System Caches
  - Level 1 Instruction and Data Caches
  - Concept
  - Organization
  - Cache Operation and programming
- Level 2 Cache Organization and Operation
- Memory Management Unit (MMU)
  - Concept
  - MMU Architecture
  - Address Translation
  - Protection
  - Table-walk
  - System Operation and Programming
- System Clock Generation
  - Clocks and Reset Sources
  - System Clock Distribution
  - PLL Programming and Operation
- Low Power Modes
- External Interfaces
  - M4IF - Multi-master Multi-Memory Interface
  - Wireless Interface (WIEM)
  - NAND Flash Controller
  - DDR
  - Advance Technology Attachment (ATA)
- System Boot
  - Internal RAM and Boot ROM
  - Graphics Memory
  - Red Boot
- IC Identification Module (IIM)
- Video and Graphics
  - IPU Overview and Basic Operation
  - Video Capturing
  - Preprocessing
  - Resizing
  - De-blocking and De-ringing
  - Color Space Conversion
  - Inversion and Rotation
- Graphic Processing Unit
  - MIPI HSC
- More i.MX51 Peripherals
  - SIM
  - USB and PHY Interface
  - MIPI SLIMBUS

## ARM / i.MX 51

HILF!GmbH Microcomputer-Consulting, Bajuwarenring 17, 82041 Oberhaching/München  
Tel.: +49 (89) 61 37 90 - 0, Fax: +49 (89) 62 52 14 5

Web: [www.hilf.de](http://www.hilf.de)  
Email: [info@hilf.de](mailto:info@hilf.de)

- |   |   |
|---|---|
| <ul style="list-style-type: none"><li>• Application Processor Peripherals<ul style="list-style-type: none"><li>• External Interrupts</li><li>• KeyPad Port</li><li>• Real-time Clock</li><li>• Pulse Width Modulator (PWM)</li><li>• General Purpose Timer (GPT)</li><li>• Enhanced Periodic Interrupt Timer</li><li>• Watchdog Timer</li></ul></li><li>• I/O Muxing<ul style="list-style-type: none"><li>• GPI/O</li><li>• Pin Assignments and Configuration</li></ul></li><li>• Audio Muxing</li><li>• Sony Phillips Digital Interface (SPDIF)</li><li>• Smart Direct Memory Access Controller (SDMA)<ul style="list-style-type: none"><li>• Overview</li><li>• Concept</li><li>• Shared Resources</li><li>• Programming Model</li><li>• I/O Requests</li><li>• Operation</li><li>• Programming</li></ul></li></ul> | <ul style="list-style-type: none"><li>• Shared Peripherals<ul style="list-style-type: none"><li>• CSPI and eCSPI</li><li>• UARTs</li><li>• SSI</li><li>• IIC</li><li>• HS IIC</li><li>• FIR</li><li>• O-WIRE</li></ul></li><li>• Power Management IC and Connectivity</li><li>• Demo using PDK Evaluation Board</li><li>• Summary</li></ul> |
|---|---|